2 W, Filterless, Class-D Stereo Audio Amplifier

SSM2306

FEATURES

Filterless Class-D amplifier with built-in output stage
2 W into 4 Ω and 1.4 W into 8 Ω at 5.0 V supply
Ultralow idle current with load resistance
>87% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
Better than 96 dB SNR (signal-to-noise ratio)
Available in 16-lead, 3 mm × 3 mm LFCSP
Single-supply operation from 2.5 V to 5.0 V
20 nA ultralow shutdown current
Short-circuit and thermal protection
Pop-and-click suppression
Built-in resistors reduce board component count
Default fixed 18 dB gain and user-adjustable

APPLICATIONS

Mobile phones
MP3 players
Portable gaming
Portable electronics
Educational toys
Notebook computers

GENERAL DESCRIPTION

The SSM2306 is a fully integrated, high efficiency, Class-D stereo audio amplifier designed to maximize performance for portable applications. The application circuit requires minimum external components and operates from a single 2.5 V to 5.0 V supply. It is capable of delivering 2 W of continuous output power with less than 10% THD + N driving a 4 Ω load from a 5.0 V supply.

The SSM2306 features ultralow idle current, high efficiency, and a low noise modulation scheme. It operates with >87% efficiency at 1.4 W into 8 Ω from a 5.0 V supply and has a signal-to-noise ratio (SNR) that is better than 96 dB. PDM modulation offers lower EMI radiated emissions compared to other Class-D architectures.

The SSM2306 has a micropower shutdown mode with a typical shutdown current of 20 nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin.

The architecture of the device allows it to achieve a very low level of pop and click to minimize voltage glitches at the output during turn-on and turn-off, thereby reducing audible noise on activation and deactivation. The fully differential input of the SSM2306 provides excellent rejection of common-mode noise on the input. Input coupling capacitors can be omitted if the dc input common-mode voltage is approximately $V_{DD}/2$.

The SSM2306 also has excellent rejection of power supply noise, including noise caused by GSM transmission bursts and RF rectification.

The SSM2306 has a preset gain of 18 dB that can be reduced by using external resistors.

The SSM2306 is specified over the commercial temperature range (−40°C to +85°C). It has built-in thermal shutdown and output short-circuit protection. It is available in a 16-lead, 3 mm × 3 mm lead frame chip scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

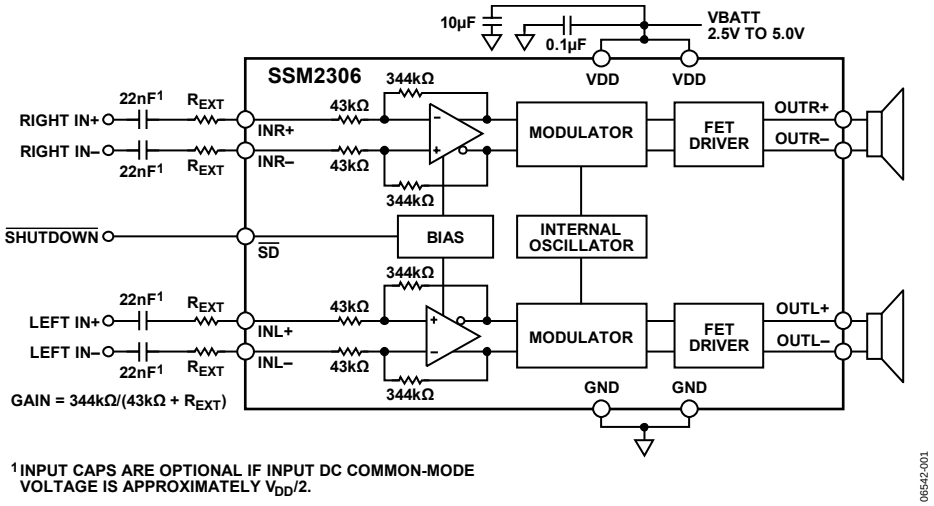

Figure 1.

Rev. 0

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REVISION HISTORY

4/07—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V; T_A = 25°C; R_L = 4 Ω, 8 Ω; gain = 6 dB, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.8		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.4		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.9		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.615		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.35		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.275		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		2.4		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.53		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.1		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.77		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.45		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 2.5 V		0.35		W
Efficiency	η	P_{OUT} = 2 W, 4 Ω, V_{DD} = 5.0 V		75		%
		P_{OUT} = 1.4 W, 8 Ω, V_{DD} = 5.0 V		85		%
Total Harmonic Distortion + Noise	THD + N	P_O = 2 W into 4 Ω each channel, f = 1 kHz, V_{DD} = 5.0 V		0.4		%
		P_O = 1 W into 8 Ω each channel, f = 1 kHz, V_{DD} = 5.0 V		0.02		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} – 1	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz, G = 18 dB, input referred		70		dB
Channel Separation	X_{TALK}	P_O = 100 mW, f = 1 kHz		78		dB
Average Switching Frequency	f_{SW}			420		kHz
Differential Output Offset Voltage	V_{OOS}			2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.0	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV rms at 217 Hz, inputs ac GND, C_{IN} = 0.1 µF, input referred		75		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		6.5		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		5.7		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		5.1		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN						
Closed-Loop Gain	A_v	R_{EXT} = 0		18		dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = VDD		43		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} ≥ 1 mA		1.2		V
Input Voltage Low	V_{IL}	I_{SY} ≤ 300 nA		0.5		V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		30		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	O_{UT}	$\overline{SD}$ = GND		>100		kΩ
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, inputs are ac-grounded, A_V = 18 dB, R_L = 4 Ω, A weighting		44		µV
Signal-to-Noise Ratio	SNR	P_{OUT} = 2.0 W, R_L = 4 Ω		96		dB

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead, 3 mm × 3 mm LFCSP	44	31.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

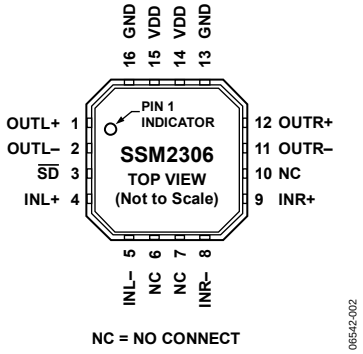

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUTL+	Inverting Output for Left Channel.
2	OUTL–	Noninverting Output for Left Channel.
3	$\overline{SD}$	Shutdown Input. Active low digital input.
4	INL+	Noninverting Input for Left Channel.
5	INL–	Inverting Input for Left Channel.
6	NC	No Connect.
7	NC	No Connect.
8	INR–	Inverting Input for Right Channel.
9	INR+	Noninverting Input for Right Channel.
10	NC	No Connect.
11	OUTR–	Noninverting Output for Right Channel.
12	OUTR+	Inverting Output for Right Channel.
13	GND	Ground for Output Amplifiers.
14	VDD	Power Supply for Output Amplifiers.
15	VDD	Power Supply for Output Amplifiers.
16	GND	Ground for Output Amplifiers.

TYPICAL PERFORMANCE CHARACTERISTICS

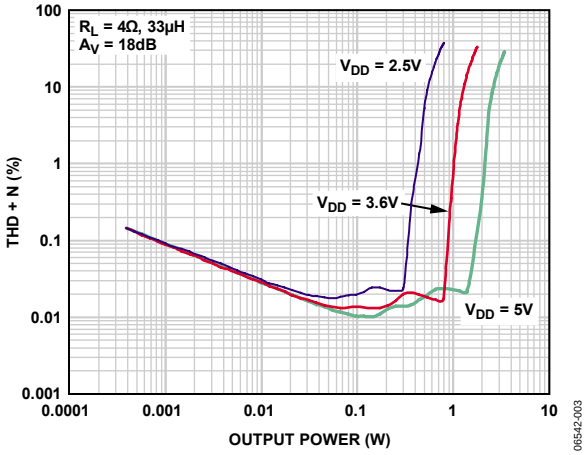

Figure 3. THD + N vs. Output Power into 4 Ω, A_V = 18 dB

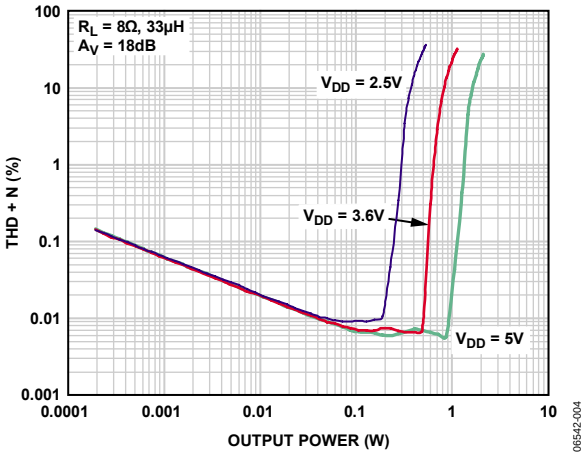

Figure 4. THD + N vs. Output Power into 8 Ω, A_V = 18 dB

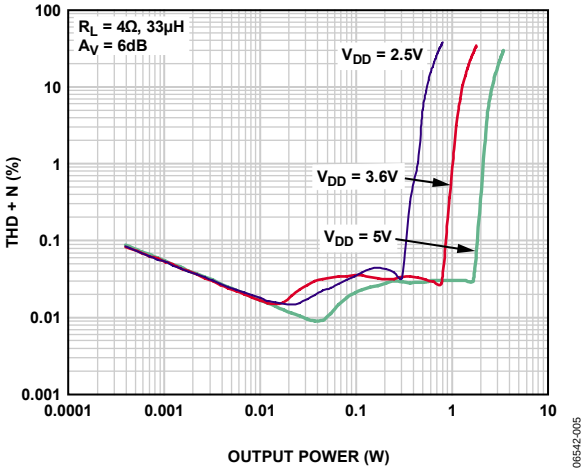

Figure 5. THD + N vs. Output Power into 4 Ω, A_V = 6 dB

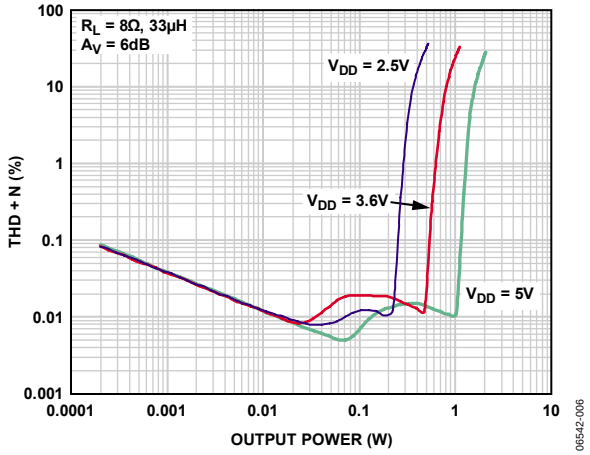

Figure 6. THD + N vs. Output Power into 8 Ω, A_V = 6 dB

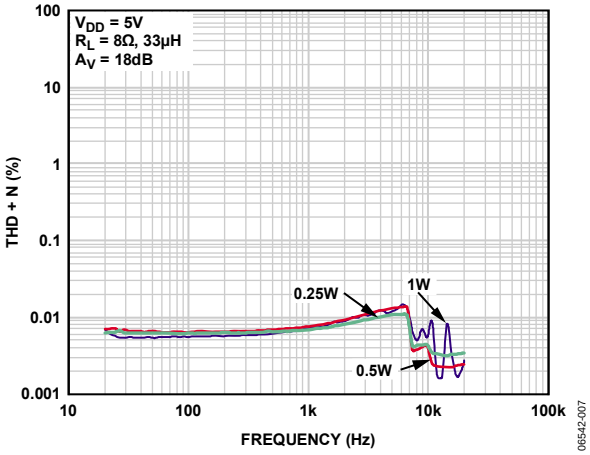

Figure 7. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω, A_V = 18 dB

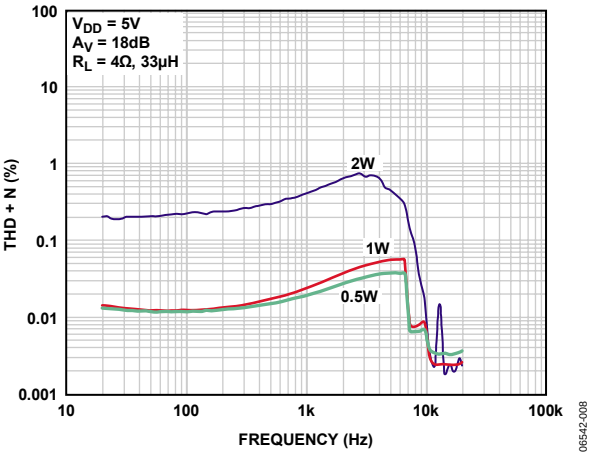

Figure 8. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω, A_V = 18 dB

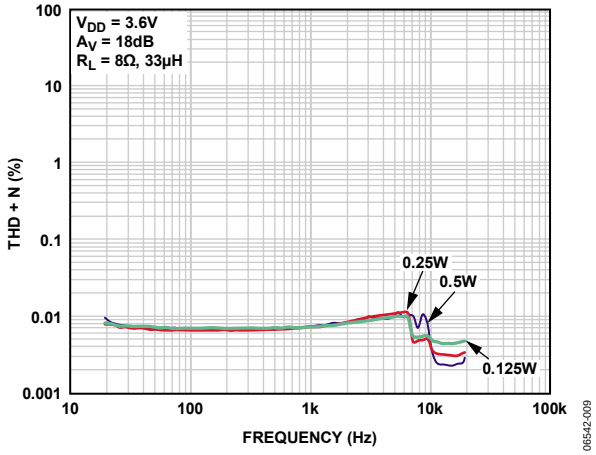

Figure 9. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω, A_V = 18 dB

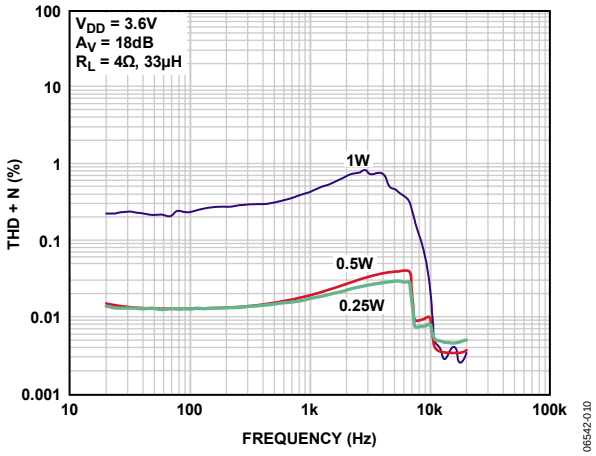

Figure 10. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω, A_V = 18 dB

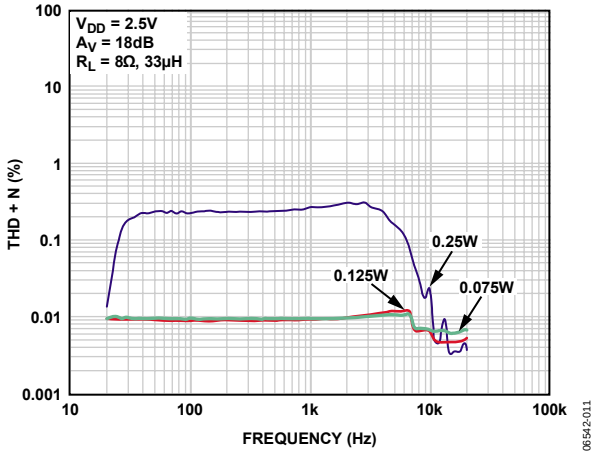

Figure 11. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω, A_V = 18 dB

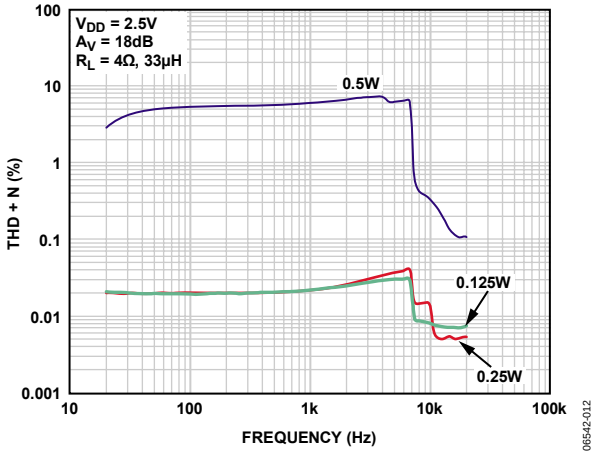

Figure 12. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω, A_V = 18 dB

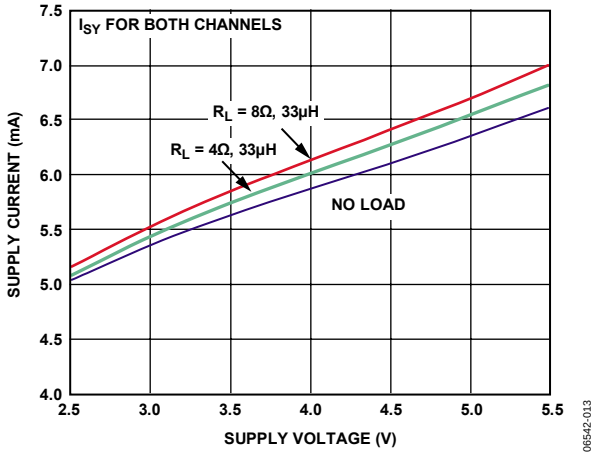

Figure 13. Supply Current vs. Supply Voltage, No Load

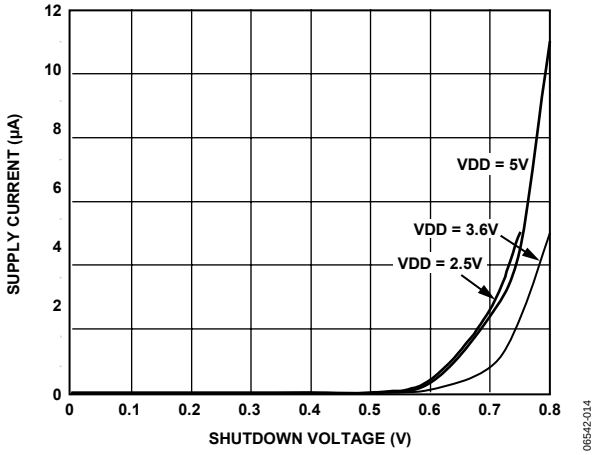

Figure 14. Supply Current vs. Shutdown Voltage

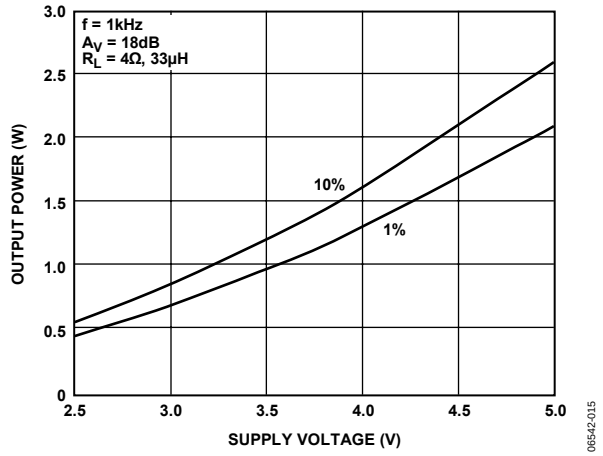

Figure 15. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, A_V = 18 dB

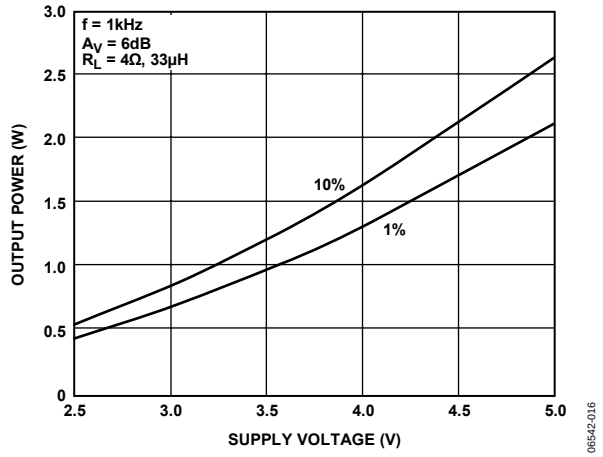

Figure 16.Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, A_V = 6 dB

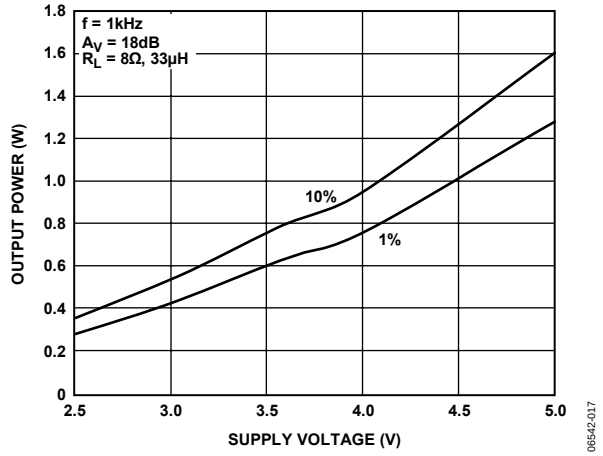

Figure 17. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, A_V = 18 dB

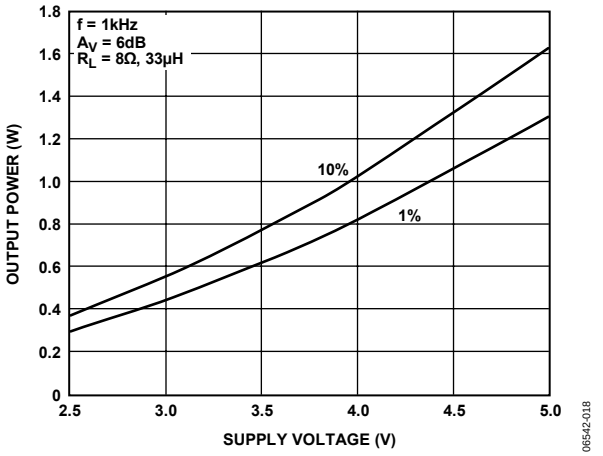

Figure 18. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, A_V = 6 dB

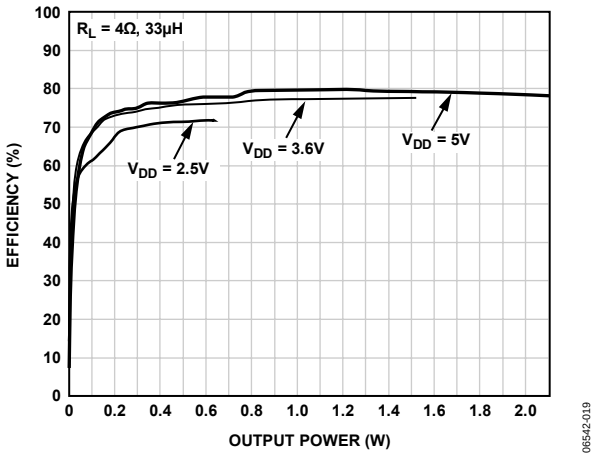

Figure 19. Efficiency vs. Output Power into 4 Ω

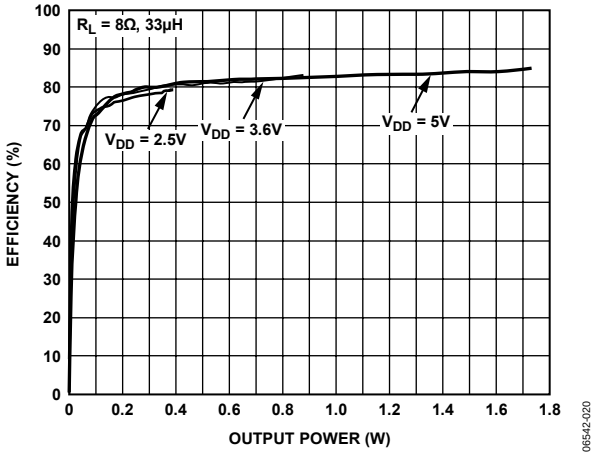

Figure 20. Efficiency vs. Output Power into 8 Ω

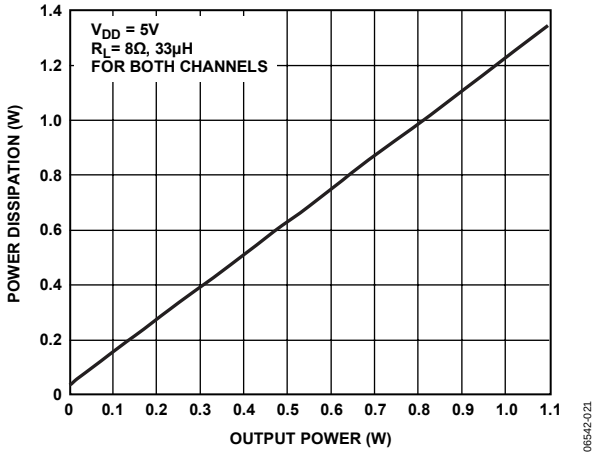

Figure 21. Power Dissipation vs. Output Power at V_{DD} = 5 V, R_L = 8 Ω

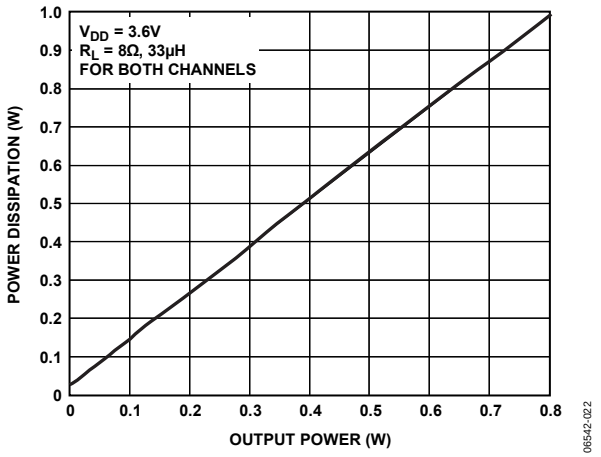

Figure 22. Power Dissipation vs. Output Power at V_{DD} = 3.6 V, R_L = 8 Ω

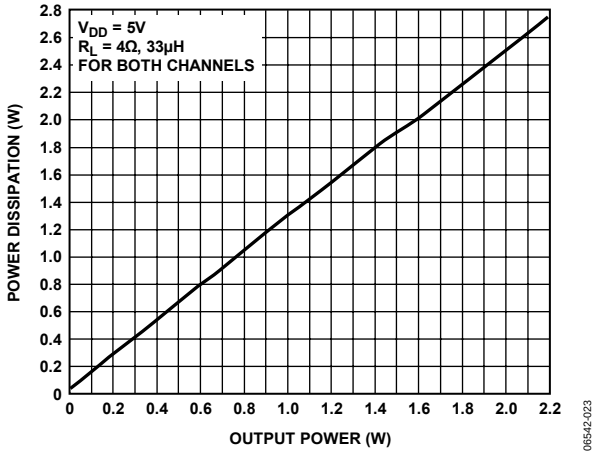

Figure 23. Power Dissipation vs. Output Power at V_{DD} = 5 V, R_L = 4 Ω

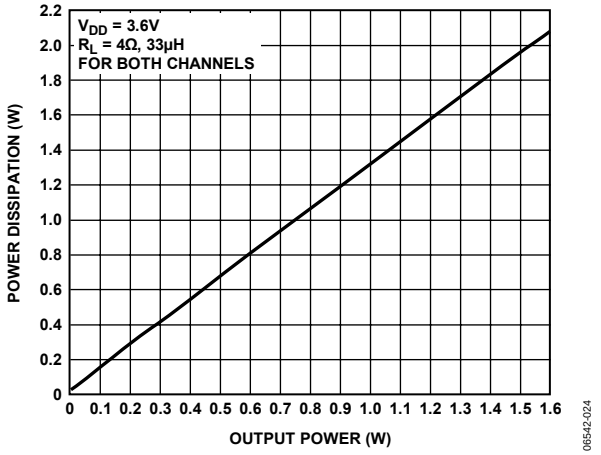

Figure 24. Power Dissipation vs. Output Power at V_{DD} = 3.6 V, R_L = 4 Ω

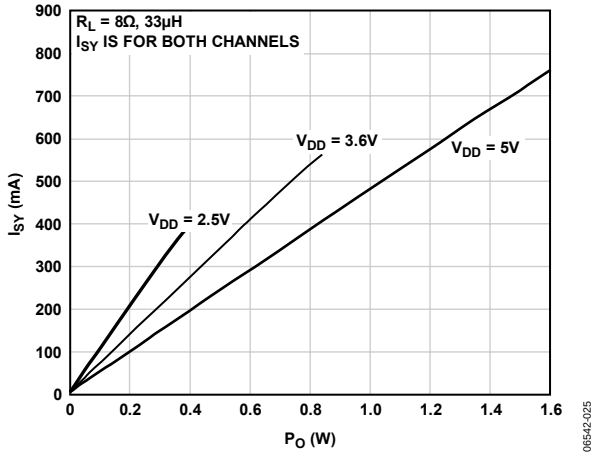

Figure 25. Supply Current vs. Output Power into 8 Ω

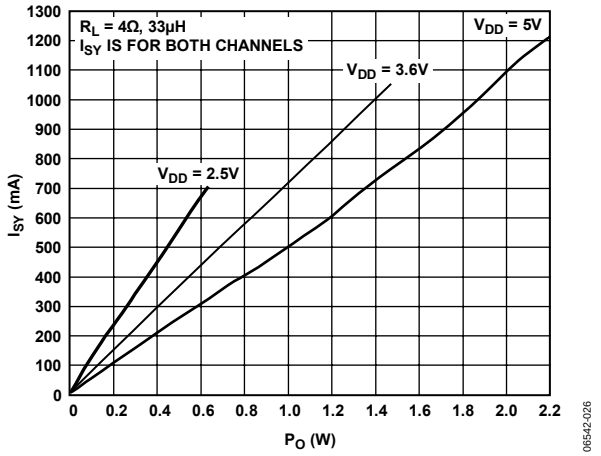

Figure 26. Supply Current vs. Output Power into 4 Ω

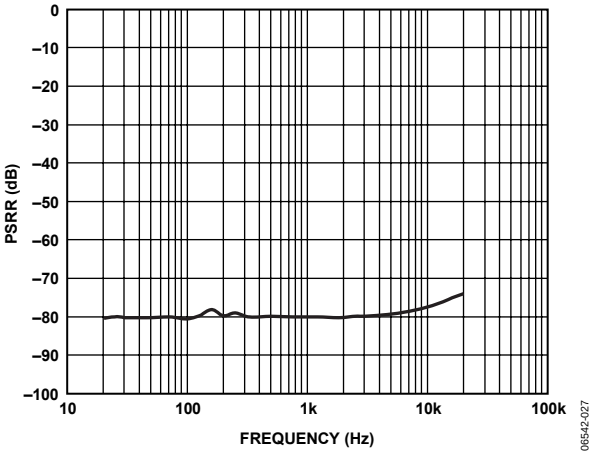

Figure 27. PSRR vs. Frequency

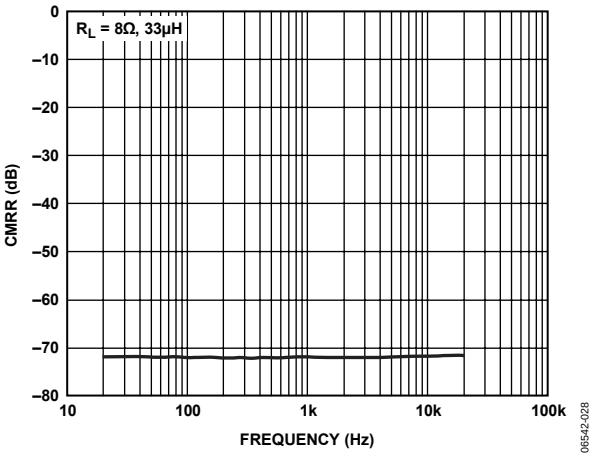

Figure 28. CMRR vs. Frequency

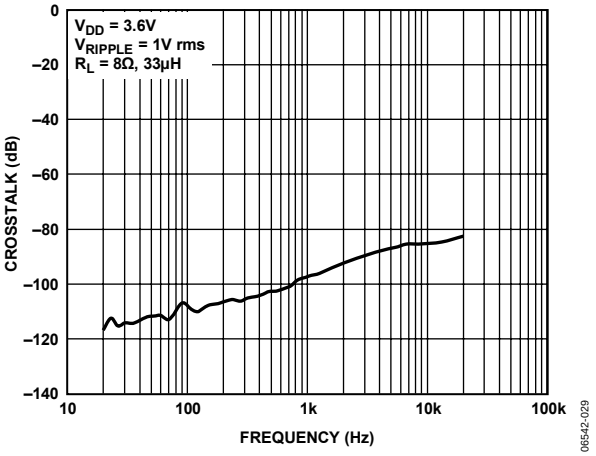

Figure 29. Crosstalk vs. Frequency

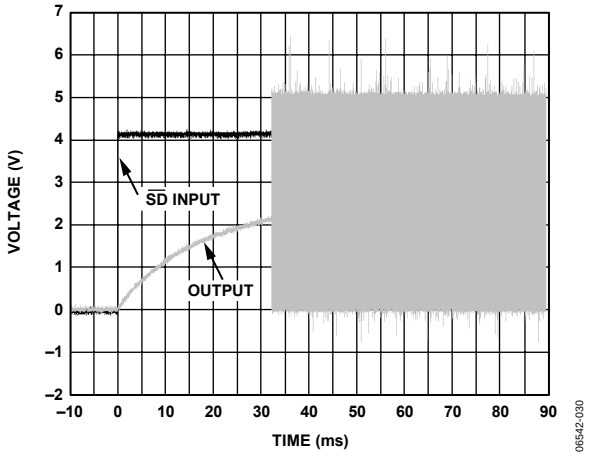

Figure 30. Turn-On Response

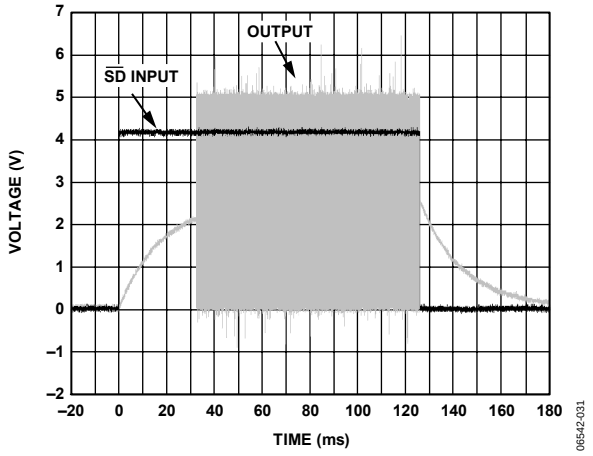

Figure 31. Turn-Off Response

TYPICAL APPLICATION CIRCUITS

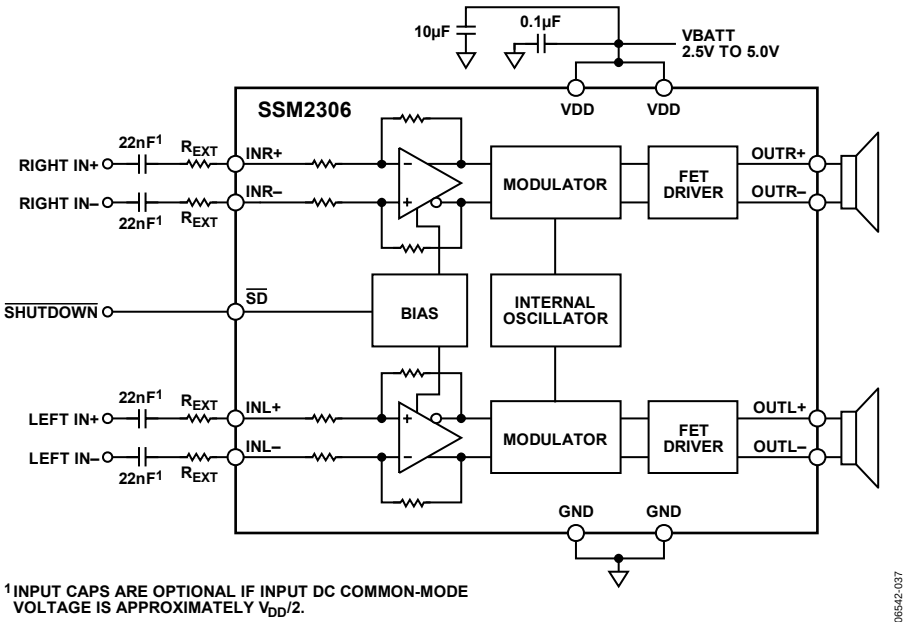

Figure 32. Stereo Differential Input Configuration

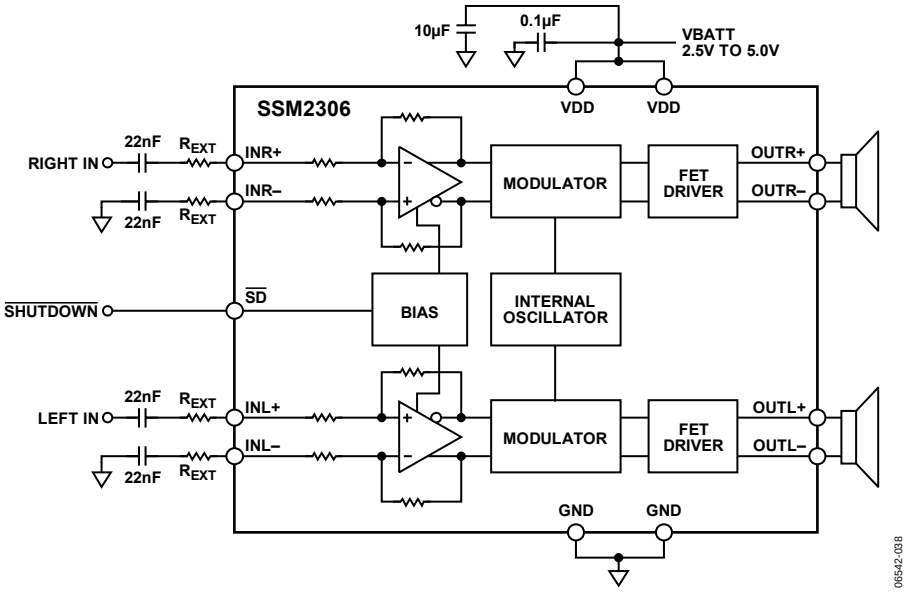

Figure 33. Stereo Single-Ended Input Configuration

APPLICATION NOTES

OVERVIEW

The SSM2306 stereo, Class-D, audio amplifier features a filterless modulation scheme that greatly reduces the external components count, conserving board space and, thus, reducing systems cost. The SSM2306 does not require an output filter; instead, it relies on the inherent inductance of the speaker coil and the natural filtering capacity of the speaker and human ear to fully recover the audio component of the square wave output.

Although most Class-D amplifiers use some variation of pulse-width modulation (PWM), the SSM2306 uses sigma-delta (Σ-Δ) modulation to determine the switching pattern of the output devices. This provides a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies; that is, reducing EMI emission that might otherwise radiate by the use of speakers and long cable traces. The SSM2306 also offers protection circuits for overcurrent and overtemperature protection.

GAIN SELECTION

The SSM2306 has a pair of internal resistors that set an 18 dB default gain for the amplifier. It is possible to adjust the SSM2306 gain by using external resistors at the input. To set a gain lower than 18 dB, refer to Figure 32 for the differential input configuration and Figure 33 for the single-ended configuration. Calculate the external gain configuration as

$$External\ Gain\ Settings = 344\ k\Omega/(43\ k\Omega + R_{EXT})$$

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur with the activation or deactivation of shutdown. Furthermore, voltage transients as low as 10 mV are audible as an audio pop in the speaker. Likewise, clicks and pops are classified as undesirable audible transients generated by the amplifier system, and as such, as not coming from the system input signal. These types of transients generate when the amplifier system changes its operating mode. For example, the following can be sources of audible transients:

- System power-up/power-down
- Mute/unmute
- Input source change
- Sample rate change

The SSM2306 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

EMI NOISE

The SSM2306 uses a proprietary modulation and spread-spectrum technology to minimize EMI emissions from the device. Figure 34 shows SSM2306 EMI emission starting from 100 kHz to 30 MHz. Figure 35 shows SSM2306 EMI emission from 30 kHz to 2 GHz. These figures clearly depict the SSM2306 EMI behavior as being well below the FCC regulation values, starting from 100 kHz and passing beyond 1 GHz of frequency. Although the overall EMI noise floor is slightly higher, frequency spurs from the SSM2306 are greatly reduced.

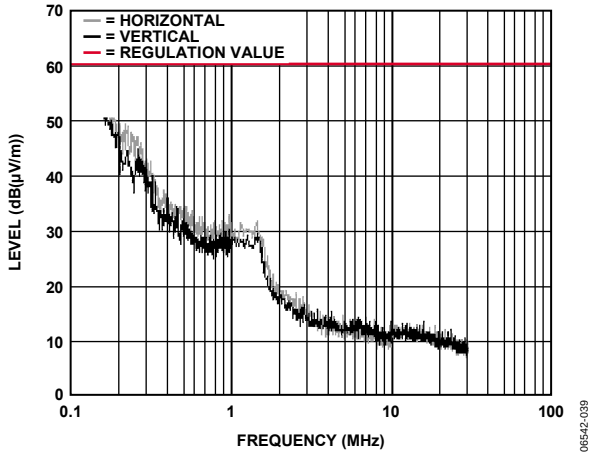

Figure 34. EMI Emissions from SSM2306

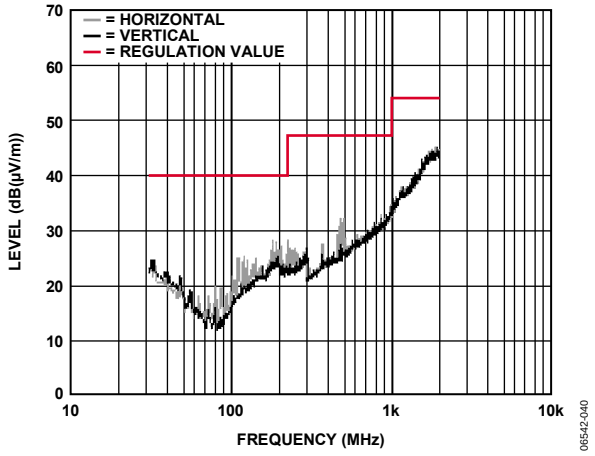

Figure 35. EMI Emissions from SSM2306

The measurements for Figure 34 and Figure 35 were taken with a 1 kHz input signal, producing 0.5 W output power into an 8 Ω load from a 3.6 V supply. Cable length was approximately 5 cm. To detect EMI, a magnetic probe was used touching the 2-inch output trace to the load.

LAYOUT

As output power continues to increase, careful layout is needed for proper placement of PCB traces and wires between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Make track widths at least 200 mil for every inch of track length for lowest DCR, and use 1 oz. or 2 oz. of copper PCB traces to further reduce IR drops and inductance. Poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal.

To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended to use a large area ground plane for minimum impedances.

Good PCB layouts isolate critical analog paths from sources of high interference; furthermore, separate high frequency circuits (analog and digital) from low frequency ones. Properly designed multilayer printed circuit boards can reduce EMI emission and increase immunity to RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossover. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and, similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes or analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2306 does not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed (see Figure 32), or if using a single-ended source (see Figure 33). If high-pass filtering is needed at the input, the input capacitor together with the input resistor of the SSM2306 form a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

Input capacitors can have very important effects on the circuit performance. Not using input capacitors degrades the output offset of the amplifier as well as the PSRR performance.

PROPER POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. Although the actual switching frequency can range from 10 kHz to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input needs to be decoupled with a good quality, low ESL and low ESR capacitor, usually around 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transients noises, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2306 helps maintain efficiency performance.

OUTLINE DIMENSIONS

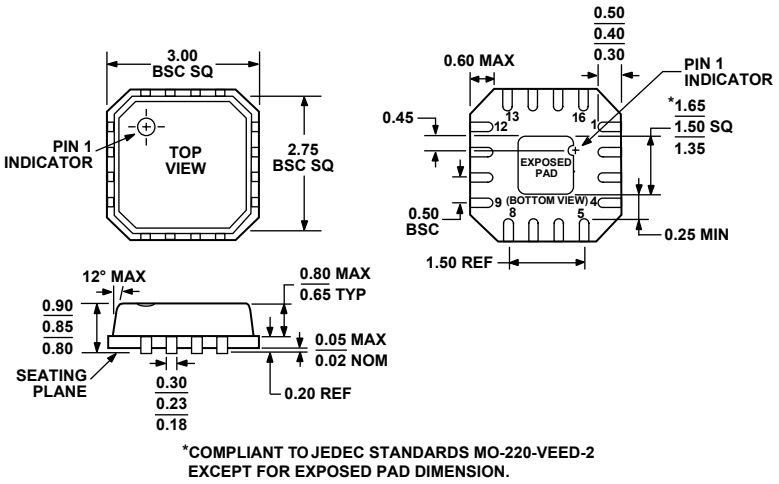

Figure 36. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
SSM2306CPZ-R2[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	A1R
SSM2306CPZ-REEL[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	A1R
SSM2306CPZ-REEL7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-3	A1R

[1] Z = RoHS Compliant Part.

NOTES

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